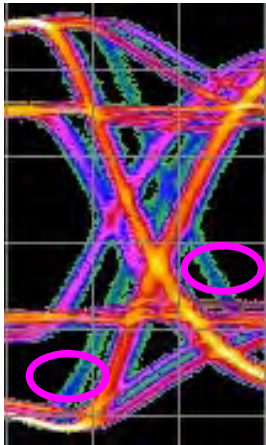


Measurement Brief: Signal Integrity of Reference Clock Bleed-Through in an IC

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 March 2006
 SR-TN056



Abstract

This paper examines some signal integrity examples related to AMB testing, but also with wider applicability. Clock bleed-through is examined, as well as the effect of a lowered supply voltage on error performance. The latter is a classic example of why eye diagrams cannot be relied upon as the sole measure of system performance.

Clock Bleed-Through Example

The following discussion is based on measurements given in Figure 1. Note that the measurements were taken directly from the output of an IC with de-emphasis switched on, giving the characteristic eye shape seen in these measurements. After the appropriate amount of travel through a dispersive medium, such as a circuit board, the signal would look like a normal NRZ eye.

	Clean	Reference Clock Bleed-Through
Eye Diagram		

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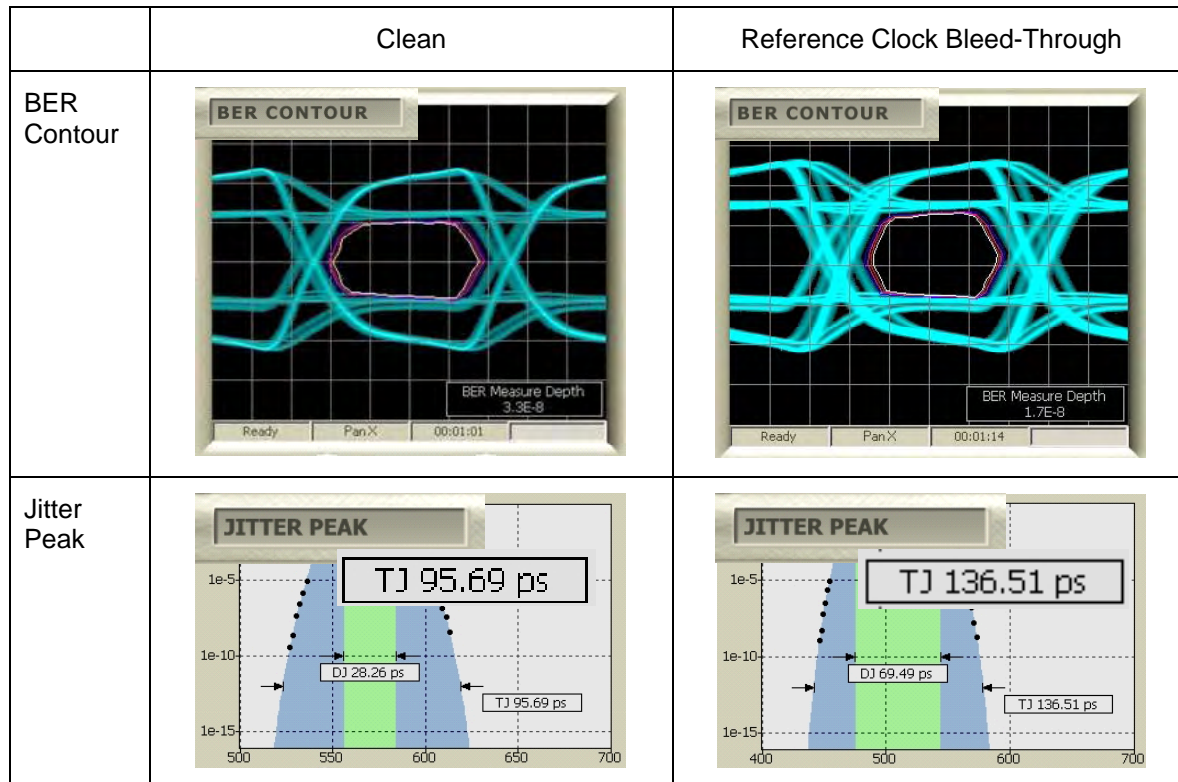


Figure 1: Comparing signal integrity measurements between a clean signal and one exhibiting clock bleed-through. Note the extra traces in the eye diagram transition (indicated with purple circles in the top right diagram). Note also that the bleed-through causes an increase in jitter (lower two measurements).

The measurements on the right column of Figure 1 were taken from an early design prototype chip. For comparison purposes, measurements from a later version of the chip are given on the left.

The first clue that the situation was not as intended are given by the jitter measurements shown at the bottom of Figure 1. The earlier part exhibits considerably more jitter than the design target. It can be seen from this that the problem seems to be mainly a DJ (Deterministic Jitter) problem. The BER Contour shows that in both cases, this is not a noise-related problem, and there are no rare events lurking – the contour lines are closely grouped and the center of the eye is quite open, again aligning with the conclusion that this is a deterministic effect. The major clue derives from the eye diagram, where there are mysterious extra traces apparent in the eye compared to its companion on the left (as indicated by the purple circles on the magnified portion of the eye). These traces are happening frequently (they must be to appear in an eye diagram) but obviously less frequently than the main data edges. The mystery edges also seem to be synchronous with the data edges, and timed with the data transitions.

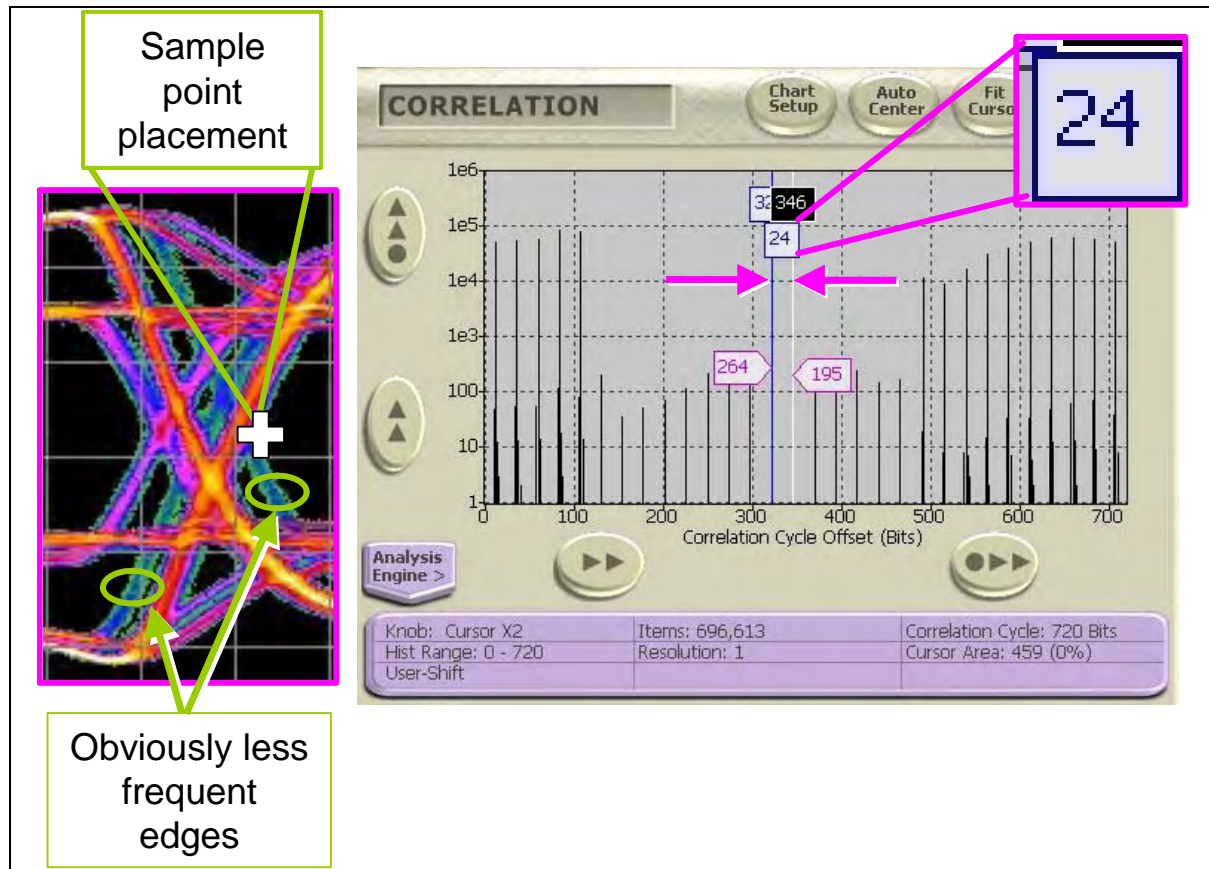


Figure 2: *Placing the BERTScope sampling point where it starts to intersect with one of the mystery edges allows use to error analysis. This shows a connection to errors occurring every 24 data bits.*

Moving the BERTScope sampling point, it is possible to explore the less frequently occurring edges (see Figure 2). Using error analysis, it becomes obvious that there is a relationship between errors, and the data rate divided by 24. For this system, this happens to correspond to the reference clock rate ($\div 24$) and turned out to be the cause.

The design was changed to increase isolation between clock and data paths, with the obviously improved performance seen in the measurements in the left column of Figure 1.

Summary

We've looked at a semiconductor chip suffering from reference clock bleed-through, and seen symptoms visible in signal integrity measurements that helped a successful redesign.