

Gigabit Signal Integrity Creates New Challenges

By Guy Foster, info@synthesysresearch.com, VP Outbound Marketing. SyntheSys Research Inc.

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It is well documented that many parallel data transfer architectures used in computing have switched over to higher speed serial data streams at Gigabits/sec. Examples include graphics card data (PCI to PCI Express) and storage communications (Parallel ATA to Serial ATA). The telecommunications industry has dealt with these higher speeds for a lot longer, but has not been forced to meet such stringent cost constraints. By engineering down to a competitive price, serial bus standards do not enjoy use of exotic microwave materials, nor are they allowed significant performance margins to make links work. A decade or two ago, signals with these frequency components would have been carried in waveguides, but to pass them across the types of circuit board materials of an average motherboard, engineers have had to get creative.

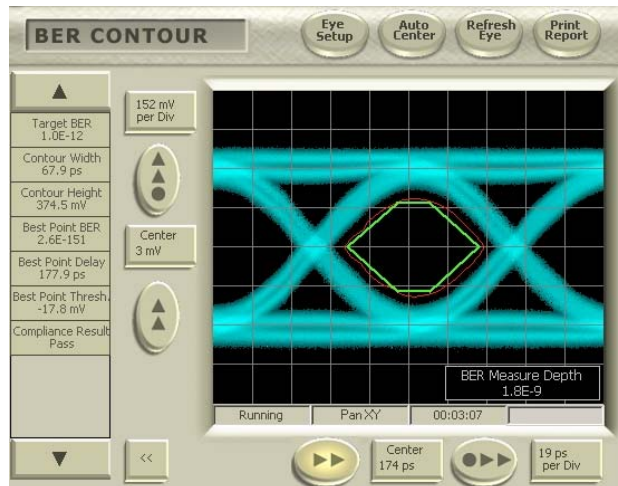
The Implications for Test

As is usual, testing falls into two main types:

- Compliance
- Troubleshooting

Transmitter Compliance Testing

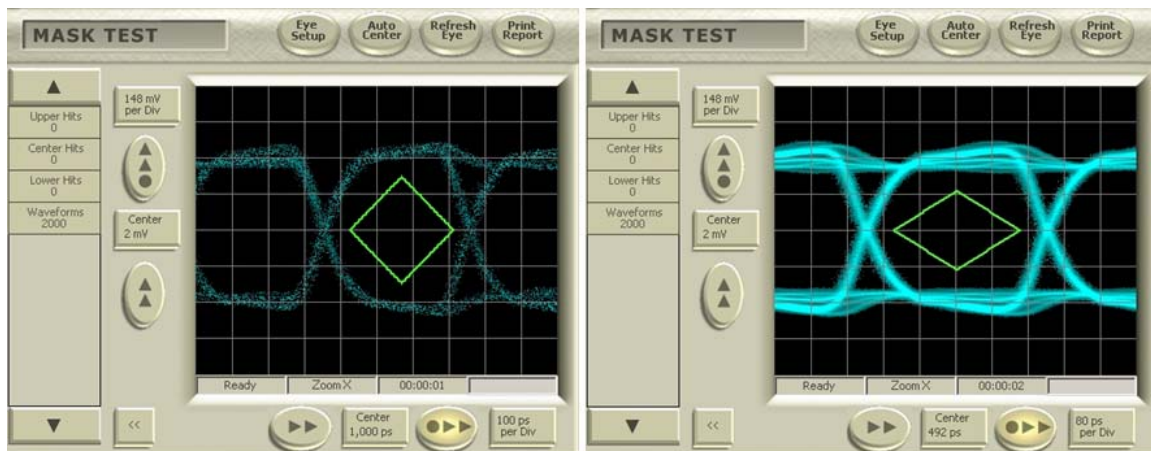
The nature of compliance testing is changing as the signals evolve and available margins are reduced. Gigabit transmitter compliance testing has traditionally been carried out through use of a sampling scope eye diagram mask as shown in Figure 1. However, these have proven to be inadequate predictors of system performance and it is increasingly common for standards to require a mask to be passed at the BER level that the system is expected to achieve. This is beyond the ability of a simple sampling scope mask to verify.



Compliance Mask Test to Assure Performance to 1×10^{-12} BER

Figure 1 - BER Based Eye Diagram Mask

A second area of interest in transmitter testing relates to the ingenuity of techniques used to overcome low cost circuit board materials. It is increasingly common for transmitter output stages to boost the high frequency content of the signal in order to overcome frequency dependent loss resulting from the material. With such de-emphasized signals the first bit of a sequence of identical bits is at a higher amplitude than subsequent bits, and requires separate mask tests for the first bit and subsequent de-emphasized bits. See Figure 2.



Transition bit mask test

Deemphasized bit mask test

Figure 2 a) Transition bit mask test and b) Deemphasized bit mask test

Receiver Compliance Testing

Changes are also occurring in receiver testing. Although in telecoms it has been traditional to test the clock recovery function of a receiver with sinusoidal jitter, serial buses have mainly avoided testing the receiver whenever possible. As rates in that arena reach 5 Gb/s, such avoidance is no longer an option. Whereas telecom testing focused on

testing the clock recovery function of a receiver only, recent standards are also requiring that the decision function be tested through the addition of other eye closure elements to form an often complex stressed eye test recipe. See a typical equipment set up for receiver compliance testing in Figure 3.

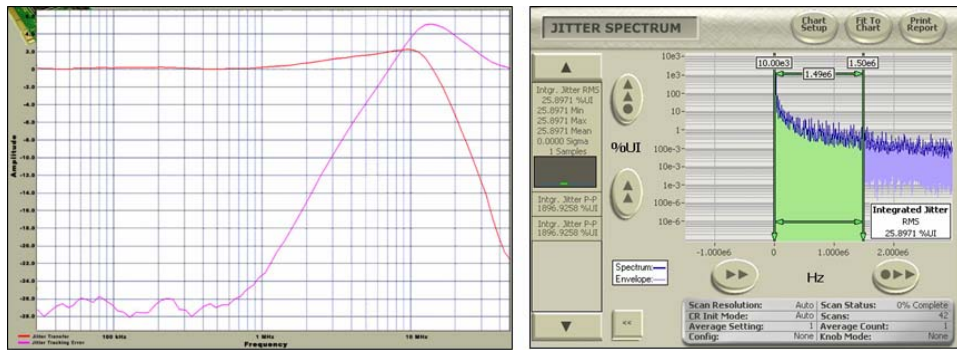


PCI Express Gen 2 Receiver Stress Setup

Figure 3 – Typical Receiver Stress Setup

Clocking Schemes

Another area that is getting more focus is clock distribution for serial bus architectures. Gigabit telecom links have traditionally used an embedded clock scheme with each data stream having dedicated clock recovery. Computer standards have employed this architecture, but also forwarded and distributed clock systems. For these latter schemes, different test methods are required. One key parameter for schemes where a low speed (e.g. 100MHz) clock is multiplied up to Gb/s rates is to measure the Phase Locked Loop, PLL, bandwidth and peaking. As many motherboards have hostile environments that cause the incoming clock to be ‘dirty’, the multiplier’s ability to reduce jitter is important and needs to be measured accurately. It is also useful to measure the jitter spectrum of clock and data to measure spectrally banded jitter values to aid troubleshooting. See Figure 4.

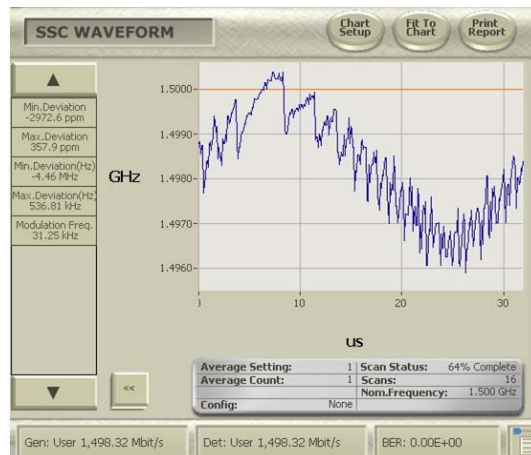


Measured PCI Express Clock Multiplier Jitter Transfer Function

Gb/s Data Rate Jitter Spectrum with Spectrally Integrated Jitter Measurement

Figure 4 – a) PCI Express Clock Multiplier Jitter Measurement, b) Spectrally Integrated Jitter Measurement for Gb/s Data Rate

A final note on clocking is the now well known use of spread spectrum clocking (SSC) to circumvent FCC regulations on interference, shown in Figure 5. The idea is that dithering the system clock frequency with a ~30kHz modulation reduces the measured emissions, even though the instantaneous power is unchanged. Our experience of measuring devices equipped with SSC is that this can be a common source of compliance test failures. It is therefore useful to be able to examine the behavior of the modulation directly to verify performance.



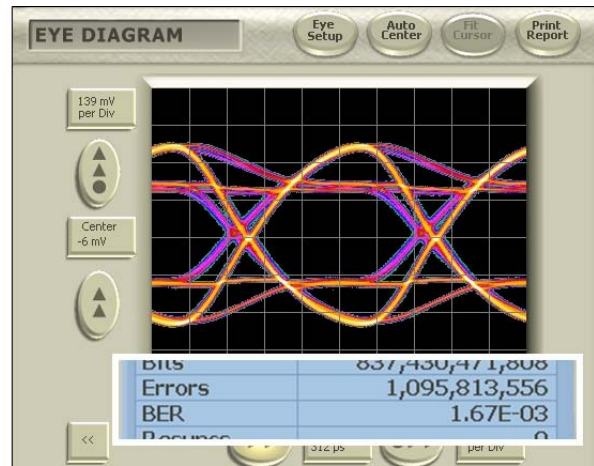
Measured SSC Waveform from Commercial Serial ATA Disk Drive

Figure 5 - Spread Spectrum Clocking (SSC) Waveform Measurement

Troubleshooting

In the early stages of designing a new product, and later if compliance issues are discovered, the ability to dig deeper is vital. We have come across numerous examples where bit error ratio (BER) measurement has been essential to uncovering the whole picture. One example is of a memory IC that developed problems when the test process exercised its ability to deal with a lowered power supply voltage. An internal logic block

started to fail at reduced voltage, but the chip's output stage continued to function correctly. The result was an output waveform that was unchanged, and the fact that the perfectly formed eye diagram was composed of bits that were just plain wrong would never have been visible in a scope-only measurement. See Figure 6. Similarly, we have helped customers making stressed eye measurements with alternative solutions track back the causes of their device failures to their test equipment being overstressed – another example of the value of measurement depth.



Eye Diagram Showing Pre-Emphasis and Healthy Eye Opening but Poor BER Performance

Figure 6 – Poor BER Performance Invisible on an Eye Diagram

Summary

As the cost-sensitive computing industry joins the telecoms sector in employing Gb/s data rates, the nature of testing is evolving to cope with the unique requirements of this segment. We've looked at some of those changes to compliance testing, and briefly touched on the topic of troubleshooting. More detail on all of the above, and also details of products that enable such testing are available on www.bertscope.com.

Guy Foster
VP Outbound Marketing
SyntheSys Research Inc.
3475-D Edison Way
Menlo Park, CA 94025
Telephone: +1 (650) 364-1853
info@synthesysresearch.com